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# SURFACE VEHICLE INFORMATION REPORT

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## CHRYSLER SENSOR AND CONTROL (CSC) BUS MULTIPLEXING NETWORK FOR CLASS 'A' APPLICATIONS

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## FOREWORD

A proprietary multiplexing technique called the Chrysler Sensor and Control (CSC) Bus has been designed which gives the systems engineer an effective means to meet the future demands of automotive customers. The CSC Bus allows the design of the base vehicle, while attaching the complete cost of optional features to the option. This paper will describe the protocol for this CSC Bus multiplexing technique and show that it leads to the simplest vehicle electronic system.

## 1. SCOPE:

The CSC Bus components defined herein were developed to provide simple, yet reliable, communication between a host master module and its sensors and actuators. The scheme chosen provides the ability to communicate in both polling mode and direct addressing modes.

### 1.1 Background:

Vehicle applications for multiplexing can be broken into three broad classifications:

a. Class A - Sensor and Control Multiplexing
b. Class B - Data Communications
c. Class C - High Speed Real Time Control

Sensor and control multiplexing is the more classical form. An example of this kind would be fluid level sensors, door/hatch switches, and control of the vehicle headlamps, tail lamps, stop lamps, horn, wipers, etc., through a multiplex wiring network. Normally, control multiplexing affects the base vehicle wiring system, which directly affects the base cost. On the other hand data communications multiplexing (Class B) interconnects intelligent modules such as the engine controller, body computer, vehicle instrument cluster, and other electronic modules. It normally does not affect the base vehicle wiring but provides an intermodule data communications link for distributed processing and, if properly partitioned, will reduce costs on all but the base vehicle. Finally, there is a class of medium to very fast real time control modules such as the engine controller, automatic transmission, and antiskid controller.

Class B multiplexing is a very useful technique for reducing the problems encountered by the automotive electronic system engineer. However, in many situations Class B multiplexing leads to a less than optimum system. This Class B network can be an effective enabler to vehicle integration but it does not solve the sensor and actuator connection problem. After a careful study of the current Class B Network, it was obvious that a different system needed to be developed. Statistically speaking, it was determined that there are approximately seven sensors to every actuator in a potential Class A multiplex network. A form of multiplexing which would permit smaller module connectors and reduce the number of wires crowding through the congested areas without introducing more modules is highly desirable. The CSC Bus is a style of multiplexing which meets these objectives.

1.1 (Continued):

Another problem presented to the system designer consists of implementing different levels of option content. Base vehicles receive limited electronic feature content, medium vehicles receive some optional electronics, and premium vehicles contain an extensive amount of electronic features. CSC multiplexing has the ability to solve this variable content uncertainty as well as the wiring congestion problem.

1.2 CSC A Potential Class A Multiplex Network:

The proposed solution defined herein integrates a multiplexer with a Hall Effect Sensing Element and replace the reed switch used in current sensors. When standard switches are given multiplexing capability they are really sensors. They no longer 'switch' as they do today. Instead they 'sense' some parameter and report back the status including sensor diagnostics. The CSC Bus allows for increased feature content in existing modules by connecting additional sensors. More exotic sensors are also practical using multiple CSC sensors.

Perhaps the biggest factor and criteria of judgment as to whether a Class A multiplexing network will be successful or not is cost. The CSC sensors have been designed to include the multiplex circuit integrated with the Hall Effect Device in the same TO92 size package. The multiplexer portion is very small and requires approximately 300 logic gates.

2. REFERENCES:

2.1 Applicable Documents:

SAE J1850, Class B Data Communications Network

R. Vig and T. Wroblewski, "Addressable Single Wire Magnetic Sensor IC for Multiplexed Control," 3rd International Conference "Automobile Electronics - Interface and Environment," SIA. Toulouse, France; April 1988

T. Wroblewski, "A Multiplexed Automotive Sensor System," Sensors, February 1989

U. Kiencke, S. Dais, and M. Litshel, "Automotive Serial Controller Area Network," SAE Technical Paper Series, International Congress and Exposition, February 1986

D. J. Arnett, "A High Performance Solution for In-House Networking - Controller Area Network (CAN)," SAE Technical Paper Series, Earth-Moving Industry Conference, April 1987

T. Wroblewski, "A SC Bus Multiplexing Technique Which Allows for Common Electronic Modules," Paper 89123, 20th ISATA, Florence, Italy; May 1989

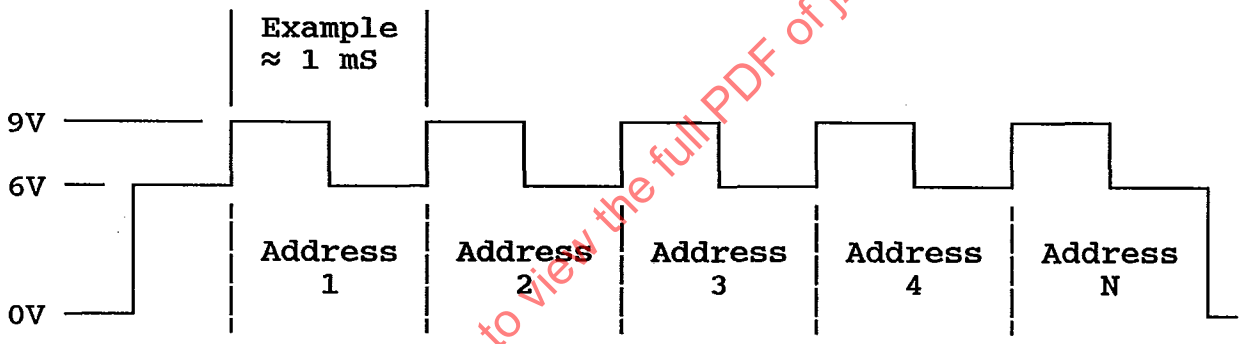
3. PROPOSED PROTOCOL:

The network method for this communication system is a master-slave polling and/or direct address method. The master uses a voltage waveform to communicate to the sensors and actuators. A sensor is addressed through successive, ordered polling of each address (time slot or period) in ascending order.

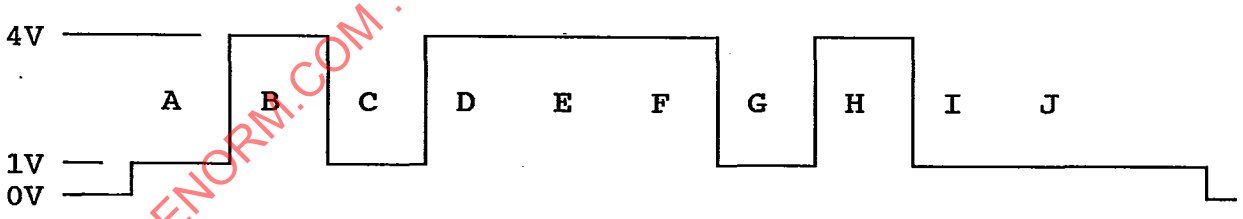
<SOM>, Wake-Up Period, Addr 1, Addr 2, ..., Addr 32

An actuator may be controlled by either the polling mode above or the direct-address, command-mode message below. The 'start of message', (SOM), is defined as the rising edge from 0 V to 6 V in the voltage waveform of Figure 1.

<SOM>, <Five-Bit address>, <1 to N data bits>, {<parity bit>}




a. CSC Bus Sensor Polling Mode Voltage Waveform




b. Voltage Representing Current Drawn by the CSC Sensors

A: Sensor Power Current
B: Sensor Presence Current
C: Switch Open
D: Sensor Presence Current
E: Switch Closed
F: Sensor Presence Current
G: Switch Open
H: Sensor Presence Current
I: Switch Open
J: No Sensor Present

FIGURE 1 - CSC Bus Sensor Polling Mode Waveform

3.1 Continuous Polling Mode Sensor Multiplexing:

Sensor multiplexing was addressed first because sensors outnumber actuators in the vehicle. Figure 1 contains the typical voltage waveform used to communicate with multiplexed sensors. As shown, the sensors use current to respond back to the master which generates the voltage waveform. In this scheme, each sensor has an internal preprogrammed address. The voltage begins at a reset (0 V) level and climbs to 6 V. This initial 6 V level provides power to the sensors. During this time, the master reads the amount of current required to keep the sensors powered, called the sensor power current. At each change from 6 to 9 V, a counter contained in the sensor is incremented. The sensors are addressed consecutively so this mode of CSC Bus communication is called the 'Continuous Polling Mode'.

4. CSC BUS SENSOR COMPONENT DESCRIPTION:

Two CSC components are available as of this publication:

a. 1: CSC Bus Two-Pin Hall-Effect Sensor
b. 2: Driver/Receiver Master Interface

4.1 CSC Bus Hall Effect Sensor:

(Reference Sprague P/N UGN/UGS3055U, Data Sheet #27680)

While the voltage is at approximately 9 V, the sensors compare the value in their counter to their preprogrammed address. If a sensor detects a match between these two values, the sensor will increase the current drain on the CSC Bus. This 'response current' informs the master that a sensor has recognized its address. This condition remains until the voltage falls to about 6 V.

When the sensor being addressed detects that the voltage is below its threshold of about 7.5 V, it will determine the status of the sensing element (magnetic field detecting Hall effect sensor, optical sensor, or mechanical switch to ground). If the sensing element is active (a magnetic field is detected, light is detected, or a mechanical switch to ground is closed), the sensor continues to draw the response current so that the master can sense the sensor's status. If the sensing element is not active, response current will cease and only the sensor power current will be drawn.

Each sensor is addressed in this manner until sensor address 32 has been addressed. After address 32, the voltage waveform returns to reset. The following blocks shown in Figure 2 are required to implement the CSC Bus addressable hall effect sensor:

a. Clock and Level Detector
b. Five-Bit Address Counter
c. Address Detector
d. On-Chip Power Supply
e. Constant Current Sink
f. Sensing Element

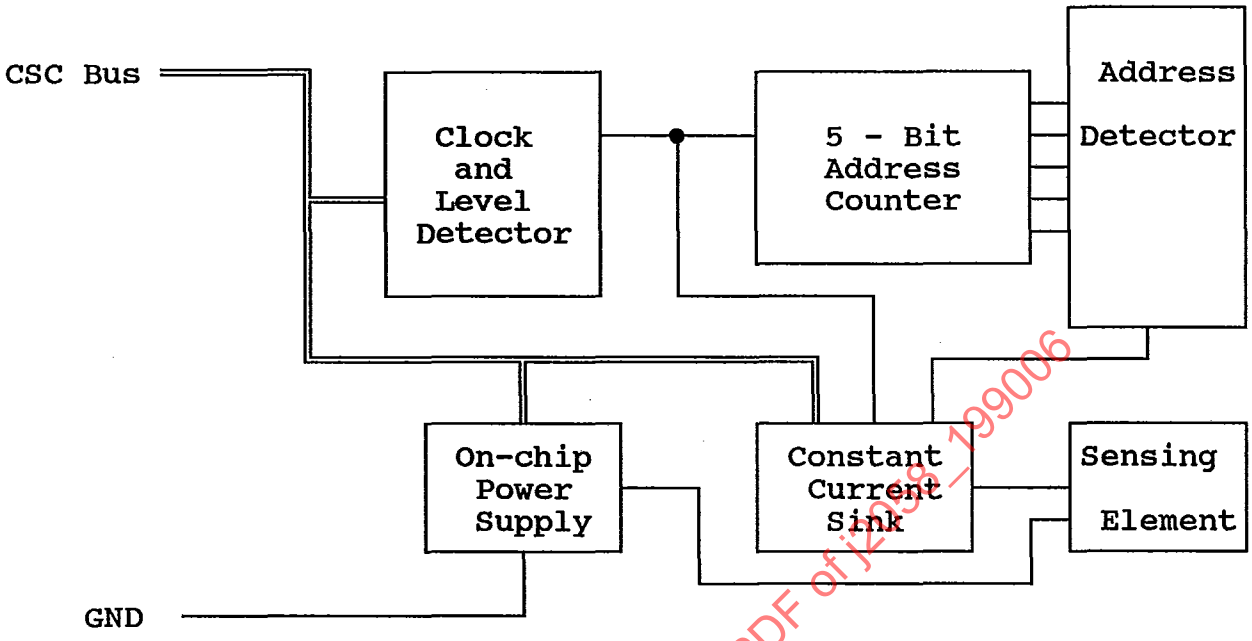



FIGURE 2 - CSC Bus Sensor Block Diagram

4.1.1 Clock and Level Detector:

The clock and level detector block contains a comparator which detects the voltage level on the CSC Bus. When the voltage rises to approximately 8 V, the comparator output becomes high and a positive signal increments the 5-bit address counter. This signal is also used in the logic to enable the constant current sink. Due to the comparator's 1-V hysteresis, the comparator waits until the voltage falls to about 7 V before its level returns low. The 1 V hysteresis prevents incorrect changes in the output of the comparator when low level oscillations are coupled to the CSC Bus line.

4.1.2 Five-Bit Address Counter:

The 5-bit address counter monitors the address period being queried by the master. The clock and level detector provides the signal which increments the counter. This counter resets each time the CSC Bus returns to the reset level (approximately 0 V).

4.1.3 Address Detector:

The address detector determines when the sensor is being addressed by the master. The particular address is determined by programming during wafer probe. When the value in the 5-bit address counter matches the programmed value, a signal is provided to enable the constant current sink.

4.1.4 On-Chip Power Supply:

The on-chip power supply provides a regulated power source for the other blocks from the changing voltage on the CSC Bus. Without a regulated supply the sensor and comparator trip levels would not be consistent.

4.1.5 Constant Current Sink:

The constant current sink is the block which contains the ability of the sensor to communicate back to the master. The current sink is enabled when the address match signal is provided by the address detector and either the bus voltage is at 9 V or a magnetic field is detected.

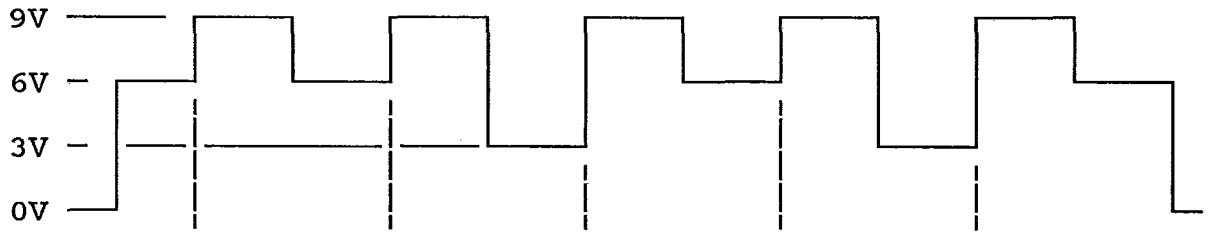
4.1.6 Sensing Element:

The sensing element acts as a switch based on some physical parameter (such as magnetic field, light level, or mechanical movement). If the proper value of the physical parameter is detected while the sensing element is powered during the 9 V section of the matched address period and is still detected during the 9 to 6 V transition, the status is latched. Once latched the status provides a signal to enable the constant current sink. Once the address in the 5-bit address counter no longer matches the programmed address, the status latch is cleared.

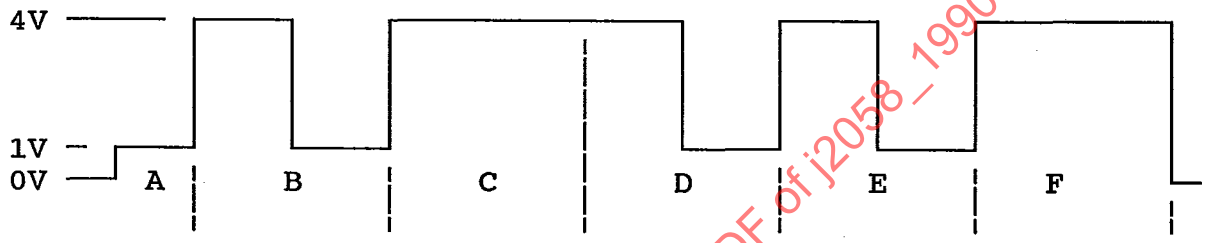
5. ACTUATOR POLLING MULTIPLEXING:

The first effort to control actuators using the CSC Bus multiplexing technique used an extension of the sensor polling mode. A particular actuator is assigned an address, just as the sensor is assigned an address (see 4.1). Each actuator monitors the CSC Bus to count the 6 to 9 V transitions in the same way as the sensor does. When the value in the counter of the actuator matches the actuator's address during the 6 V portion of the address, the actuator draws current to tell the master that the actuator is recognizing its address.

To activate an actuator output the status must first be monitored by checking the current drawn during the second half of the address cycle. In contrast to the sensor polling scheme which uses 6 V and 9 V levels only, the actuator multiplexing scheme adds a third 3 V level (see Figure 3). During the second half of the address cycle, the level is driven to 3 V by the master when the output of the actuator is to be toggled. The actuator monitors the CSC Bus during its address. If the actuator detects the 3 V level, a latch is set. The actuator does not change its output after the first 3 V level is detected because of noise considerations.




a. CSC Bus Actuator Polling Mode Voltage Waveform




b. Voltage Representing Current Drawn by Sensors and Actuators

A: Sensor Power Current
B: Sensor Present, not Active
C: Actuator Toggled, High
D: Actuator Status Presently High
E: Actuator Toggled, Low
F: Sensor Present, Active

FIGURE 3 - Continuous Polling Actuator Multiplexing Waveforms

5. (Continued):

The actuator monitors the following polling cycle. If the second half of the actuator's address period in the very next polling cycle is 3 V, then the actuator will toggle its output. Every subsequent polling cycle must contain the 6 V level during the actuator's address period for the output to remain constant. The current drawn by the actuator during this second half indicates the status of the output. When the output is to change state again, two consecutive polling cycles must contain 3 V levels during the second half of the actuator's address period.

The blocks used for this 'polling' form of actuator multiplexing shown in Figure 4 are very similar to the blocks used for the sensor shown in Figure 2. The sensing element in the sensor is replaced by a toggle latch and output latch block in the actuator. The clock and level detector block includes a 3 V level detector in the actuator that the sensor does not need. The actuator must perform properly at a 3 V level, retain information in its toggle latch and drive an output. For these reasons, the actuator does not draw its power from the multiplex link, but receives power from a dedicated 'power' input pin instead.

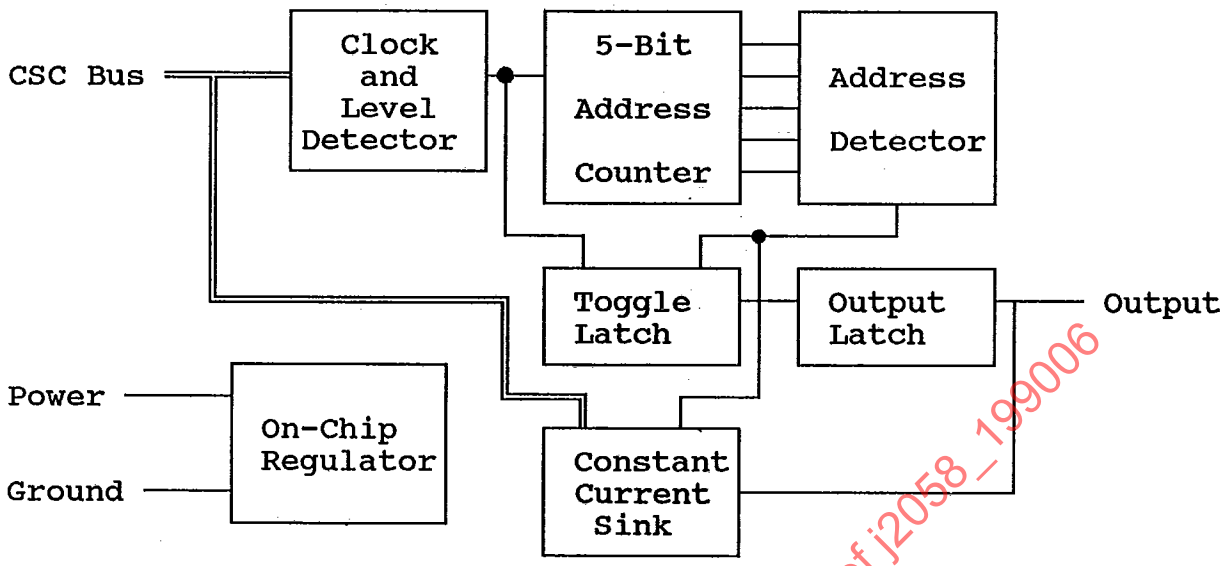
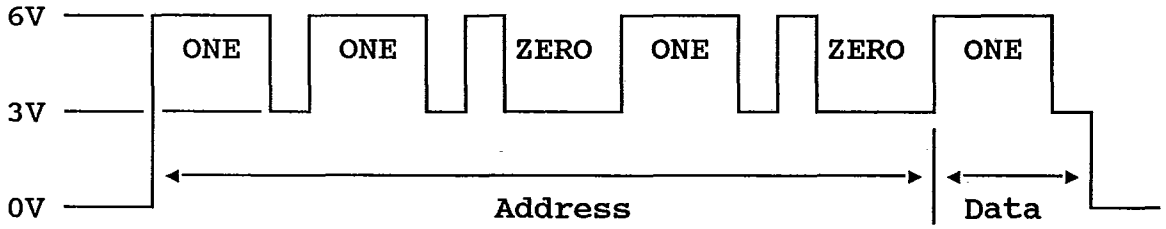



FIGURE 4 - CSC Bus Actuator Polling Block Diagram

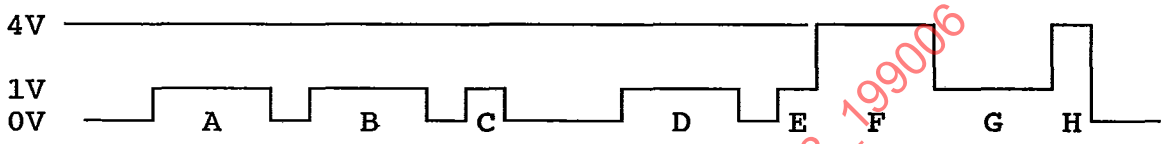
5.1 Actuator Command Mode Multiplexing:

In order to increase the flexibility of the communication scheme, the system designer has as an option a complementary actuator multiplexing capability. In order to provide all polling addresses to sensors and permit direct addressing of a particular actuator, a scheme was devised that compliments the polling mode. This scheme has been called the 'command mode', 'direct addressing' or 'control mode' of the CSC Bus.

Instead of sequentially addressing the actuators as in Method 1, the master sends a 6 ms voltage signal to the actuators (Figure 5). This waveform consists of transitions between 6 and 3 V. The example 6 ms waveform is divided into six 1 ms bits, and is called a 6-bit word. A 75%:25% pulse width modulation technique is used to define the bit value. Each bit begins with a transition to 6 V. For example a '1' bit is defined as 750 µS at 6 V and 250 µS at 3 V. A '0' bit is defined as 250 µS at 6 V and 750 µS at 3 V.




a. CSC Bus Command Mode Actuator Multiplexing Voltage Waveform




A, B, C, D, E, and G: Sensor Power Current
F: Actuator Response Current
H: Actuator Output Status High

b. Voltage Representing Current Drawn by Sensors and Actuators

FIGURE 5 - CSC Bus Command Mode Actuator Multiplexing Waveform

5.1 (Continued):

The first 5 bits of the 6-bit word are used to address the particular actuator and the sixth bit is used to control the state of the actuator's output. The master provides the voltage waveform. The CSC Bus is initially at reset (≈ 0 V). From reset, the voltage waveform is driven to 6 V. The waveform stays at 6 V for either 750 µS or 250 µS, depending on whether the bit is a one or a zero, respectively. The CSC Bus then falls to 3 V for the remainder of the 1 ms bit period. During the 6 V portion of the first bit, the master monitors the current drawn by the components on the CSC Bus. The master will use this current later as a reference to determine if an actuator has recognized its address.

All 6 bits are transmitted the same as described above. During the 3 V portion of the fifth and final address bit, the master can determine that an actuator has recognized its address by measuring the amount of current being drawn. In order to validate the proper addressing of the actuator in a noisy vehicle environment the following procedure is suggested. If this current is not above the reference current measured, no actuator is listening and there is no need to send the data bit. If two or more actuators are listening (determined by double the expected response current during the 3 V portion of the fifth address bit), the master can reset (output 0 V) the CSC Bus instead of sending the data bit to an incorrect actuator. If one actuator is listening, the master would then send the data bit (sixth and final bit in the word). During the 3 V portion of the data bit, the actuator returns the status of its output to the master by sinking the proper amount of current. If the master detects that the actuator output is not in the correct state, the command can be resent.

## 6. CSC BUS COMMAND MODE ACTUATOR:

The following blocks (Figure 6) are necessary to implement an actuator that can receive commands from the command mode of the CSC Bus and make up the parts of the command mode actuator:

a. Reset, Clock, and Level Detector
b. Integrator and Bit Value Detector
c. Shift Register
d. Bit Counter
e. Address Detector
f. Output Latch
g. Current Sink
h. On-Chip Regulator

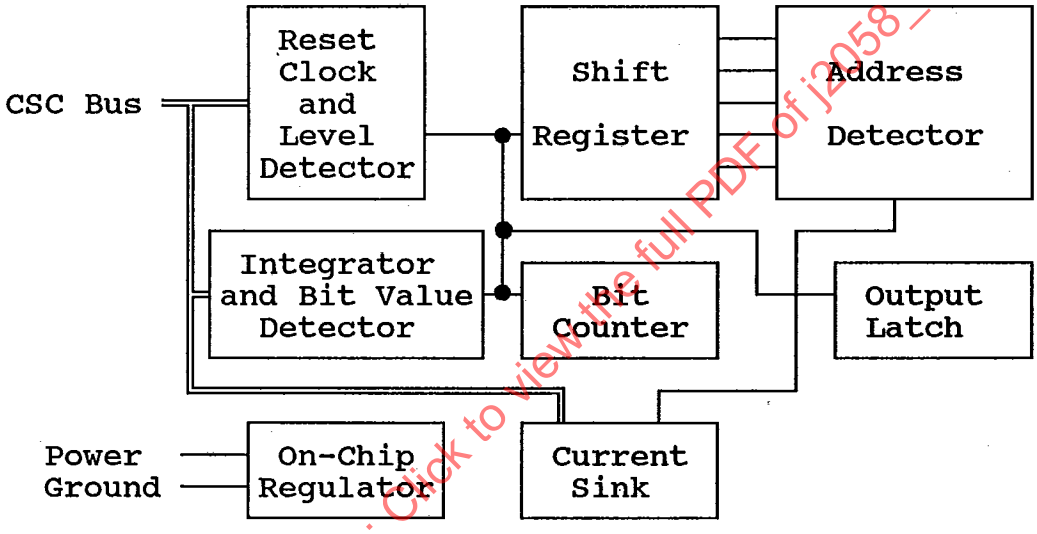



FIGURE 6 - CSC Bus Command Mode Actuator Block Diagram

### 6.1 Reset, Clock, and Level Detector:

The reset, clock, and level detector block contains the circuitry to

a. Provide a power-on reset of the output latch upon application of power
b. Provide a clock signal to the counter, shift register, and integrator and bit value detector
c. Provide a level to the address detector and current sink

### 6.2 Integrator and Bit Value Detector:

The integrator and bit value detector contains a comparator and reference to detect a one or a zero based on an external capacitor voltage charged through a resistor to the CSC Bus when the CSC Bus voltage is at 6 V. The value of the comparator is latched at the transition from 6 to 3 V. This block also provides a low impedance path from the capacitor to ground (effectively shorting the capacitor) when the CSC Bus voltage is 3 V. The output of the comparator latch is provided to the shift register and output latch.

6.3 Shift Register:

The shift register contains a 5 bit register which gets its data from the integrator and bit value detector. Data is shifted during the transition to 6 V.

6.4 Bit Counter:

The bit counter contains a 3 bit counter which is clocked during the 6 to 3 V transition. When the value is five, all address bits have been received and the address detector can compare the bits in the shift register to an internal address. If the value is six and an address match has been detected, the output of the integrator and bit value detector is latched into the output latch.

6.5 Address Detector:

The address detector detects a match between the address detected in the shift register and an internal address. If a match is detected, the current sink is enabled and the data bit from the integrator and bit value detector is clocked into the output latch.

6.6 Output Latch:

The output latch is used to latch the value of the data bit from the integrator and bit value detector at the transition from 6 to 3 V when the bit counter is six.

6.7 Current Sink:

The current sink is used to report the actuator's status to the master. If the address sent by the master matches an internal address, the current sink is enabled during the 3 V portion of the last address (fifth) bit. The current sink is also enabled during the 3 V portion of the data (sixth) bit if the output is high and the address sent matches the internal address.

7. DRIVER/RECEIVER MASTER INTERFACE:

(Referance Cherry Semiconductor P/N CS-4252)

The CSC Bus utilizes a Master - Slave protocol. This protocol is appropriate because the master is usually the present major feature module and its associated sensors and actuators are the slaves. The feature module microcomputer is the host to the driver/receiver interface IC. In many applications the module connector size is significantly reduced and the host microcomputer ROM size associated with the sensors and actuators can be reduced because software efficiency is improved. In some instances Class B multiplex slave modules can be replaced by simpler CSC Bus sensor/actuator nodes.

7. (Continued):

The CSC Bus driver/receiver master interface integrated circuit contains the circuitry required to provide a DC offset square wave output (VCSC). This output is controlled by two digital CMOS inputs, A and B. These two inputs are provided by a host microcomputer acting as the 'brains' of the master control module. The IC is able to sense the CSC Bus current and convert it to an analog voltage. This voltage is provided by the IC output (ICSC) for use by the microcomputer analogue input. The driver/receiver master interface IC has the blocks required to perform the following functions (See Figure 7):

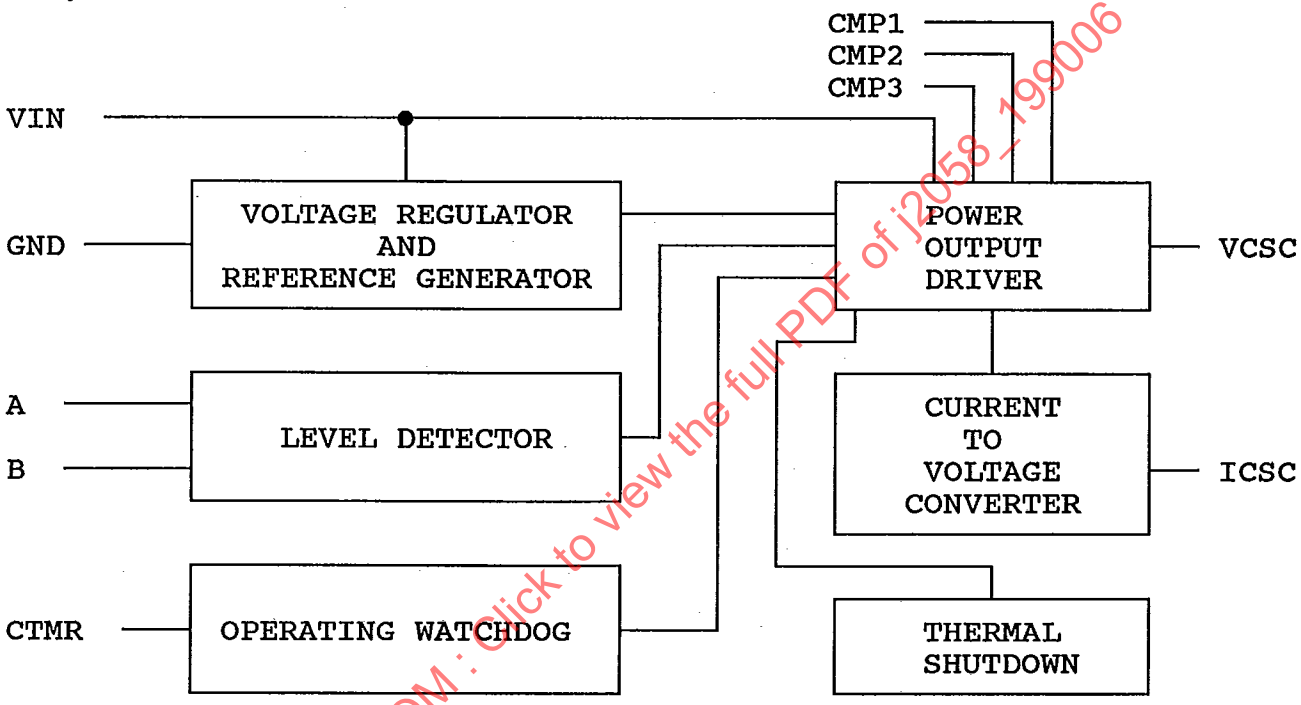
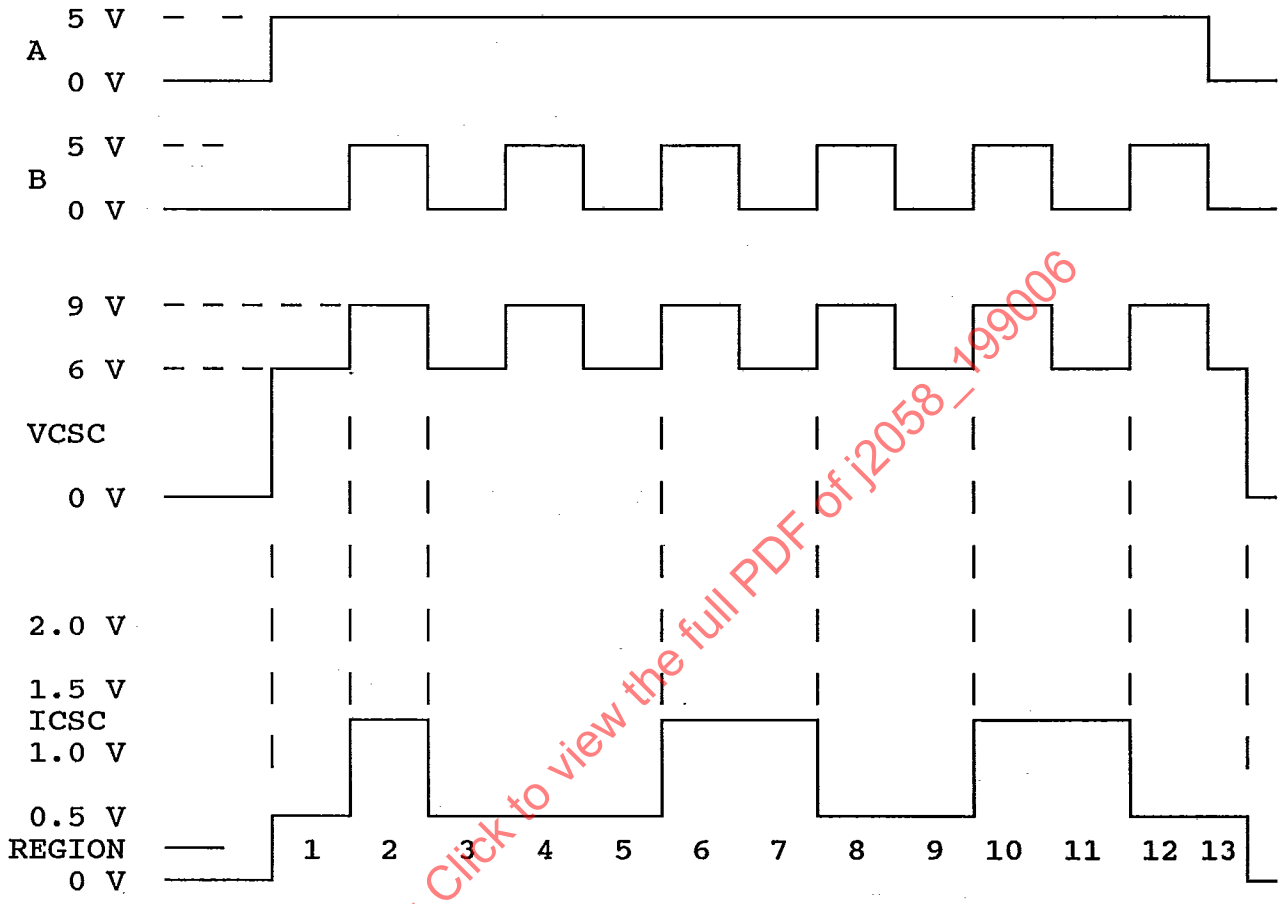



FIGURE 7 - Driver/Receiver Master Interface Integrated Circuit Block Diagram

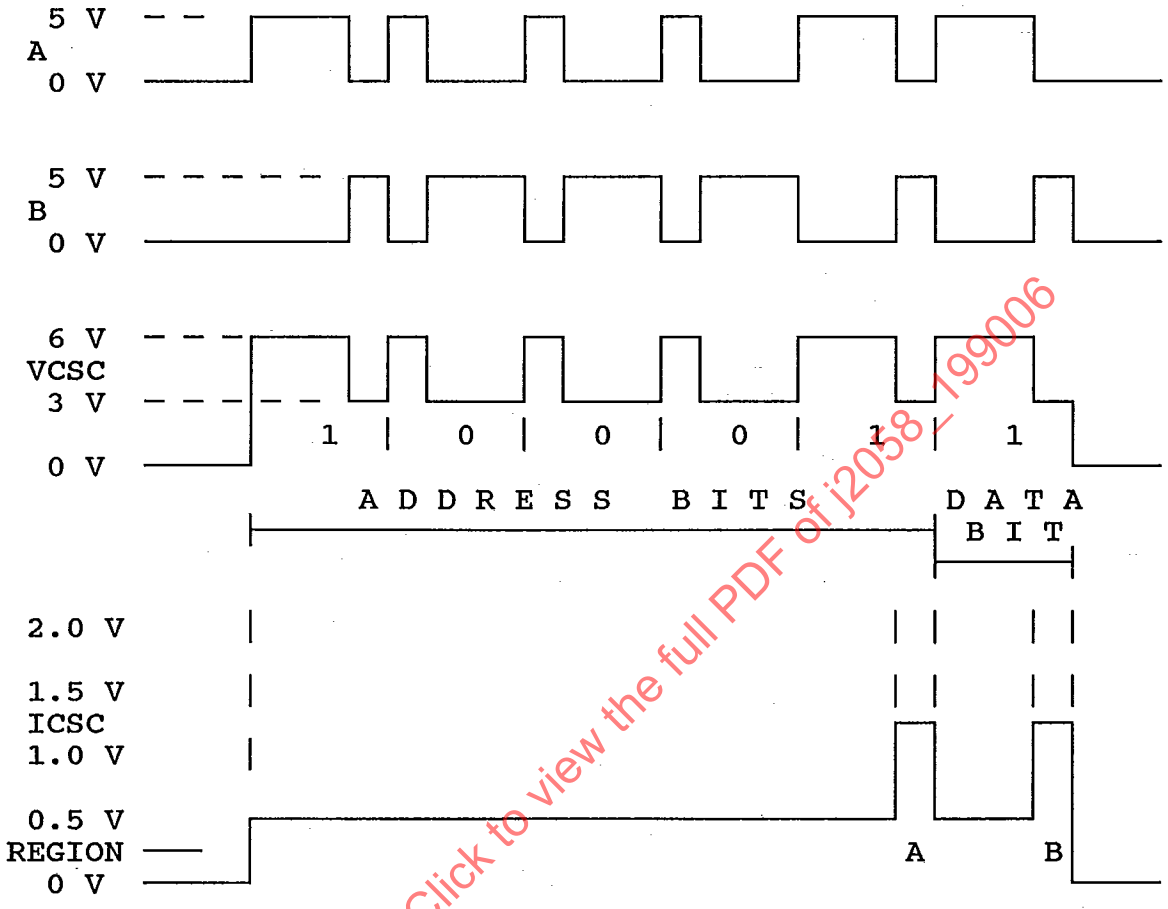
7.1 CSC Bus Output:

When A and B are both logic LOW, VCSC is OFF (RESET, approximately 0 V). When B is logic HI and A is logic LOW, VCSC is approximately 3 V. When B is logic LOW and A is logic HI, VCSC is approximately 6 V. When A and B are both logic HI, VCSC is approximately 9 V. This output is able to source 125 mA. If VIN falls below 9 V, the voltages track VIN. This output has sufficient filtering and waveshaping to keep the frequency emissions below that level which would interfere with RF communications (AM, FM, CB, etc.) through appropriate external passive networks connected to CMP1, CMP2, and CMP3. Figure 8 shows a typical continuous polling mode waveform with the A and B input pattern required to achieve this waveform. Figure 9 shows a typical command mode waveform with the A and B inputs required to realize this waveform.




| REGION | EXPLANATION |
|---|---|
| 1 | Initial voltage representing quiescent current |
| 2 | Sensor #1 PRESENT |
| 3 | Sensor #1 DOES NOT DETECT a magnet |
| 4 | Sensor #2 NOT PRESENT |
| 5 | Sensor #2 NO MEANING since sensor #2 not detected |
| 6 | Sensor #3 PRESENT |
| 7 | Sensor #3 DOES DETECT a magnet |
| 8 | Sensor #4 NOT PRESENT |
| 9 | Sensor #4 NO MEANING since sensor #4 not detected |
| 10 | Sensor #5 PRESENT |
| 11 | Sensor #5 DOES DETECT a magnet |
| 12 | Sensor #6 NOT PRESENT |
| 13 | Sensor #6 NO MEANING since sensor #6 not detected |

FIGURE 8 - Unfiltered Bus Waveform for the Continuous Polling Mode




| REGION | EXPLANATION |
|---|---|
| A | Current Feedback to Indicate Element Listening |
| B | Current Feedback to Indicate Status of Respective Output is High |

FIGURE 9 - Unfiltered Bus Waveform for the Command Addressing Mode

7.2 CSC Bus Current Mirror:

The ICSC output provides a voltage proportional to the current on the single wire CSC Bus when connected to a resistor to ground. The relationship is shown in Table 1. This output is driven to 5 V during thermal shutdown or external short circuits.

TABLE 1 - Current to Voltage Converter

| CSC Bus Current | ICSC Output (with 2.7K to Ground) | | |
|---|---|---|---|
| | MIN | TYP | MAX |
| 10 mA | 0.356 V | 0.375 V | 0.394 V |
| 20 mA | 0.712 V | 0.750 V | 0.788 V |
| 30 mA | 1.069 V | 1.125 V | 1.181 V |
| 40 mA | 1.425 V | 1.500 V | 1.575 V |
| 50 mA | 1.781 V | 1.875 V | 1.969 V |
| 60 mA | 2.137 V | 2.250 V | 2.363 V |
| 70 mA | 2.494 V | 2.625 V | 2.756 V |
| 80 mA | 2.850 V | 3.000 V | 3.150 V |
| 90 mA | 3.206 V | 3.375 V | 3.544 V |
| 100 mA | 3.562 V | 3.750 V | 3.938 V |
| 110 mA | 3.919 V | 4.125 V | 4.331 V |
| 120 mA | 4.275 V | 4.500 V | 4.725 V |
| > 133 mA | 4.730 V | 5.000 V | 5.300 V |

7.3 Operating Watchdog:

To eliminate the possibility of destroying any of the sensors if the bus gets locked at 9 V while a sensor's current sink is on, an operating watchdog disables the bus voltage. The watchdog is a timer that resets each time AB=00 is received. The timer length is determined by the charging of an external capacitor.

7.4 Thermal Shutdown:

The IC has a built-in thermal shutdown capability that disables the output if the chip temperature reaches an unsafe operating temperature.

7.5 Current Limiter:

The output device current supply is limited to 150 mA by an on-board current-limiter to prevent the destruction of the IC and a CSC Bus multiplexed smart sensor connected backwards.

7.6 Output Wave Shaper:

Passive networks connected to pins CMP1, CMP2, and CMP3 shapes the VCSC waveform to limit the amplitude of frequency components that would interfere with RF communication (AM, FM, CB, etc.). The networks limits the rise and fall times to between 10 µS and 50 µS. This network does not affect the drive capability or source impedance of the VCSC stage.