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GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETs

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GUIDELINES FOR MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETs

(From JEDEC Council Ballot JCB-86-27A, formulated under the cognizance of JC-50 Committee on Gallium Arsenide Compound Semiconductors.)

1. GENERAL

1.1 Background

For power GaAs FET applications requiring high reliability an accurate measurement of thermal resistance is extremely important to provide the user with knowledge of the FET's operating temperature so that more accurate life estimates can be made. FET failure mechanisms and failure rates have, in general, an exponential dependence on temperature (which is why temperature-accelerated testing is successful). Because of the exponential relationship of failure rate with temperature, the thermal resistance should be referenced to the hottest part of the FET. Contributions to the thermal resistance in a FET arise from several sources including (see Figure 1 for definitions; these guidelines primarily address channel-to-mounting surface thermal resistance, $R_{\theta CM}$ for GaAs MESFETs in flanged packages):

(1) the thermal conductance of the GaAs

(2) the thermal conductance of the heat sink

(3) the thermal conductance of the die attach

(4) the package (including flange and heat sink bond, if any) thermal conductance

(5) the topology of the heat generation, i.e., where the heat is generated within the FET channel.

Consequently, the thermal resistance is dependent on:

(1) the FET channel temperature

(2) the FET flange temperature (and where it is measured)

(3) the dc bias

(4) the RF operating point.

1.1 Background (continued)

Generally the largest contribution to the thermal resistance comes from the GaAs. Therefore, the magnitude of the channel temperature is of prime importance in the measurement of the thermal resistance, the other effects being secondary.

1.2 Applications

Thermal resistance measurements are made for a number of purposes. These include:

(1) die-attach screening

(2) whole-FET screening (including package)

(3) steady-state thermal resistance characterization.

Die-attach screening is relatively fast (<1 second), easy and repeatable. It is unaffected by the method used to clamp the FET's flange and is usually accomplished by the electrical technique although it is not limited to that method. The other two purposes are essentially equivalent. Since for those measurements the FET is self-heated until the channel temperature is constant they usually require heating times >1 second and demand careful attention to mounting of the FET in order to avoid errors in measured thermal resistance due to improper flange-to-test fixture mounting. This thermal resistance is the one used to estimate channel temperatures.

1.3 Measurement Techniques

Several measurement techniques for thermal resistance are in common use today. They are:

(1) Electrical, or forward V_{GS}, technique

(2) IR (infrared) technique

(3) Liquid crystal techniques

Only the first two are suitable for 100% screening and only the electrical technique is suitable for hermetically sealed packages. All techniques have the following steps in common:

1.3 Measurement Techniques (continued)

(1) A known power is input for a known period of time (or until a steady-state condition is reached)

(2) A change in channel temperature is measured

(3) The thermal resistance calculation is made.

Differences in results among the techniques arise because of differences in:

(1) Heating time

(2) Temperature measurement accuracy

(3) Temperature distribution across the FET.

The ideal thermal resistance technique would accurately measure the temperature of the hottest spot in the FET in RF operation with the FET flange being held at a constant temperature. The measurement should not affect the device's operation nor alter it in any way and should be useable on 100% of the FETs. It should be useable on hermetically sealed FETs and provide a steady-state thermal resistance. None of the present techniques meet all of these criteria. Briefly their characteristics are:

1.3.1 Electrical Technique

In this technique the change in forward-biased gate voltage (at a constant gate current) with a change in temperature is first measured. Then the change in forward-biased gate voltage ΔV_{GS}, in response to a heating pulse is measured. The thermal resistance can then be calculated. The heating pulse is obtained by applying a drain potential, V_{DS}, during the heating period. The gate may be biased either positive or negative during the heating pulse.

1.3.1 Electrical Technique (continued)

If it is positive then the drain current will be greater than I_{DSS}. If the FET has a simple gate with a uniform temperature distribution and uniform electrical characteristics along its length this technique should give accurate results. However, power FETs have many gates in parallel and the channel temperatures and electrical characteristics are typically nonuniform. Consequently, this technique provides an "average" channel temperature which is an average over the individual gate responses. A feature of the technique is that it can be applied to FETs in hermetic packages. This technique does not directly give hot-spot thermal resistance.

1.3.2 IR Technique

In this technique the circuit heat sink is held at a known temperature, a known bias is applied to the FET and the resulting temperature at any point in the FET can be determined by measuring the IR radiation from the site. Consequently, this technique can be used to determine the thermal resistance related to the hottest spot on the FET. However, the hot-spot dimension is on the order of the channel dimension (length around one micrometer for X-band FETs) while the resolution for the IR microscopes is only 15 to 30 micrometers and is not expected to improve. Therefore, the IR temperature measured is an average temperature over a 15 to 30 micrometers spatial area that includes the channel. Within these limits this technique can also be used to determine the temperature differential across the FET. Disadvantages to this technique are that the FET chip must be exposed for the measurement and regions of varying emissivity (common to upright mounted FETs) can cause additional measurement errors if not handled properly.

1.3.3 Liquid Crystal Technique

In this technique a liquid crystal is chosen which has a transition in the desired temperature range. The FET is then coated with the material and, with the circuit heat sink temperature held constant, bias power is increased until a change in polarization (seen as a dark spot) is observed on some area of the FET.

1.3.3 Liquid Crystal Technique (continued)

Since the temperature at which this change occurs is accurately known a thermal resistance can be calculated. By observing the FET under a mircoscope (using visible light) one-micrometer size features can be resolved. This technique can be used to determine hot spots and can be very accurate. It is not normally used on deliverable FETs since the FET is contaminated with the liquid crystal. Also, the FET must be visible to make the measurement so hermetic parts cannot be examined. Other disadvantages are:

(1) Only a limited temperature range of liquid crystals is available.

(2) The liquid crystal can affect the temperature distribution if improperly applied.

(3) Contamination can change the transition temperature of some liquid crystals.

All three techniques are subject to measurement and interpretational difficulties and therefore careful calibration and analysis are musts. Table 1 provides a summary of the three techniques.

A thermal resistance screen is a necessary, but not sufficient, screen for good die bonds (or source bonds for flip-chip FETs). A screen based on limiting the temperature difference between the hottest and coldest channels on the FET is also important to ensure a good bond.

With this background the following guidelines, goals and suggestions are proposed for thermal resistance measurement.

2. GUIDELINES

(1) The thermal resistance measurement technique should be applicable to deliverable parts.

(2) Steady-state, as opposed to transient, $R_{\theta CM}$ should be measured and provided for FETs intended for use in cw operation.

(3) The temperature of the mounting surface (heat sink) to which the transistor flange is attached should be held constant during the $R_{\theta CM}$ measurement.

(4) The $R_{\theta CM}$ should be measured at a channel temperature appropriate to the manufacturer's suggested application temperature. The manufacturer should also provide data indicating the expected temperature variation of the thermal resistance over the operating temperature range of FET.

(5) If a technique is used that measures $R_{\theta CM}$ prior to the completion of processing, the manufacturer should verify that the subsequent processing does not affect $R_{\theta CM}$.

(6) The manufacturer should provide or possess calibration information (for their chosen $R_{\theta CMC}$ technique) allowing correlation with other techniques.

(7) The attachment technique, including screw size (if any) and torque or clamping pressure used to attach the transistor flange to the circuit heat sink during the $R_{\theta CM}$ measurement, should be specified.

(8) The conditions (flange and channel temperatures and bias levels) used to measure $R_{\theta CM}$ should be recorded and provided for each FET measured.

(9) The temperature difference between the hottest and coldest channel should be measured at the channel temperature used in the $R_{\theta CM}$ measurement.

3. RECOMMENDATIONS

(1) Use IR technique to determine ΔT across the FET (before capping).

(2) Use electrical or IR technique to measure $R_{\theta CM}$.

(3) Use the liquid crystal technique to calibrate the IR and electrical techniques.

(4) Use pulsed electrical technique for die attach screening.

(5) The $R_{\theta CM}$ should be measured on 100% of deliverable parts intended for applications requiring high reliability.

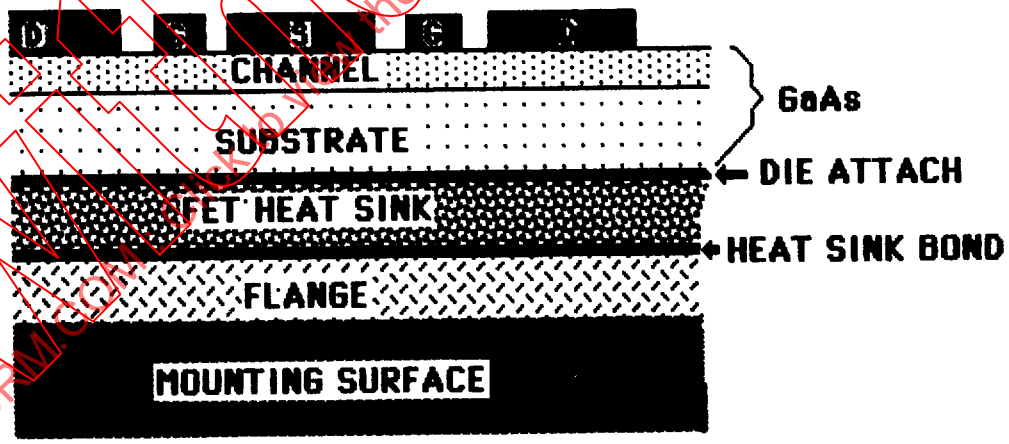

FIGURE 1

Typical Construction of Upright FET Mounted
On a Test Or Application Circuit
(D = drain, G = gate, S = source)

4. DESIRED GOALS FOR FUTURE GUIDELINES

(1) The $R_{\Theta CM}$ obtained from the hottest spot on each FET should be measured and recorded.

(2) Since the various measurement techniques for thermal resistance use approximations to the true hot-spot temperature, the manufacturer should relate the results of his $R_{\Theta CM}$ measurement to the true hot-spot temperature.

(3) The variation of $R_{\Theta CM}$ with the RF operating parameters should be determined.